Amendments to the specification

Please replace paragraph 1 on page 1 of the application with the following revised paragraph:

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of application Serial No. 10/119,458, filed April 9, 2002, now Patent No. 6,596,384.

Please replace paragraph 2 on page 6 which continues as paragraph 1 on page 7 with the following revised paragraph:

Referring now to Figures 1-3, a signal layer or plane 10 and a reference voltage layer or plane 12 are shown laminated together using a sticker sheet 13. The signal layer has signal lines 14 disposed on a dielectric material 15, such as FR4. (FR4 material is an epoxy coated fiberglass material well known in the art and can be laminated, if one of the laminates is in the partially cured condition, and then fully cured.) The signal lines, one of which is shown at 14, terminate at lands 16, which are disposed around openings at drilled and plated through holes, one of which is shown at 17 in the drawings. The signal lines have a top surface 18, a pair of side surfaces 20 and 22 and a bottom surface 24. (It is to be understood that "top" refers to the surface that is oriented away from the dielectric 15, the bottom surface 24 refers to the surface which is in contact with the dielectric 15, and the side surfaces 20 and 22 refer to those surfaces which connect the top and bottom surfaces 18 and 24.) The lands 16 each have a top roughened surface 25 which is maintained in the roughened condition, whereas the top surface and preferably the side surfaces 20 and 22 of the signal lines 14 are smooth. (The roughened surfaces in this and other figures are represented by stippling or by saw-tooth shapes, when appropriate. As used herein, the term "smooth" generally refers to an R_z measurement of less than about 1 micron. The term "rough" as used herein generally refers to a surface that has an R_z measurement of greater than about 3 microns. Mean roughness depth R_z is the arithmetic mean value of the single roughness depths R_z (i), where R_z(i) is the vertical distance between the highest peak and the deepest valley within consecutive sampling lengths. The terms "R_z" or "R_z(DIN)" are set forth in ASME B46.1-1995 or ISO 4287-1997.)

Please replace paragraph 2 on page 7 which continues as paragraph 1 on page 8 with the following revised paragraph:

The reference voltage layer 12 has a copper voltage plane 26 laminated to a dielectric material 27 which, again, preferably is FR4. Opening 28 is the location of the drilled and plated through hole formed in the composite structure, and is the same plated through hole that forms opening 17 in the signal layer. In this view, the opening 28 of the drilled and plated through hole is formed in the dielectric material 27; a larger opening 29 is etched in the voltage plane 26 during initial personalization so as to form a clearance area around the plated through hole at opening 28. The sticker sheet 13 is disposed between the signal layer 10 and the reference voltage layer 12 to which the signal layer 10 and reference voltage layer 12 are laminated by conventional means. The sticker sheet also preferably is made of FR4 material and is maintained in the B cured state (partially cured) for lamination, after which the laminate is fully cured. During drilling of holes at the composite level, opening 32 is formed through sticker 13 aligning with opening 17 in dielectric 15 and opening 28 in dielectric 27 so that a continuous through opening is provided. The openings 32, 29 and 17 provide the surface for plated through hole ~~33~~ which comprises copper plated onto the dielectric materials in a conventional manner. The land 16 is in contact with the copper plating 33 in the openings 17, 29 and 32 to provide for a signal path. The copper plating 33 includes annular collars on opposite sides of the laminate structure. (It is to be understood that the printed wiring board shown in Figures 1-3 is for illustrative purposes only and that several different layers could be, and typically are, stacked but the showing only of the layers 10 and 12 illustrates the present invention.)